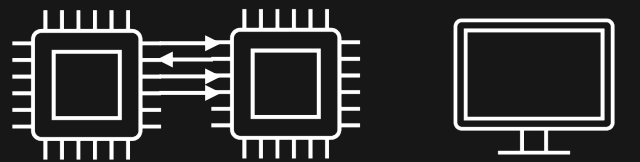
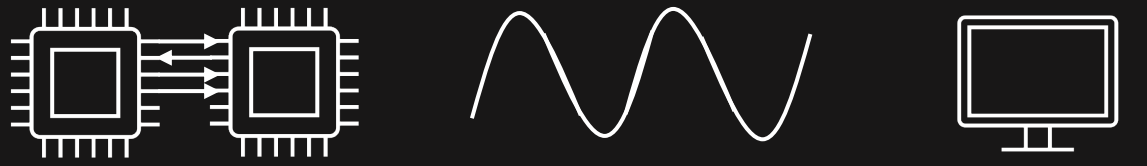
Day 3

Agenda



SPI OLED

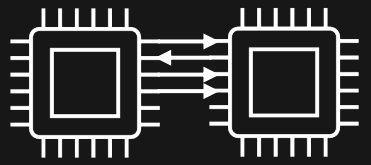
Task 1



SPI Analog to digital converter OLED

Task 2

Agenda

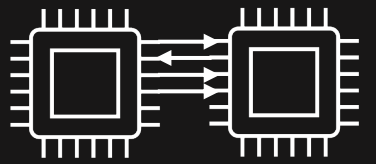


SPI

Analog to digital converter

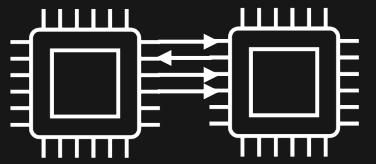
OLED

SPI – Task 1



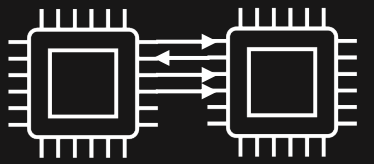
Demo

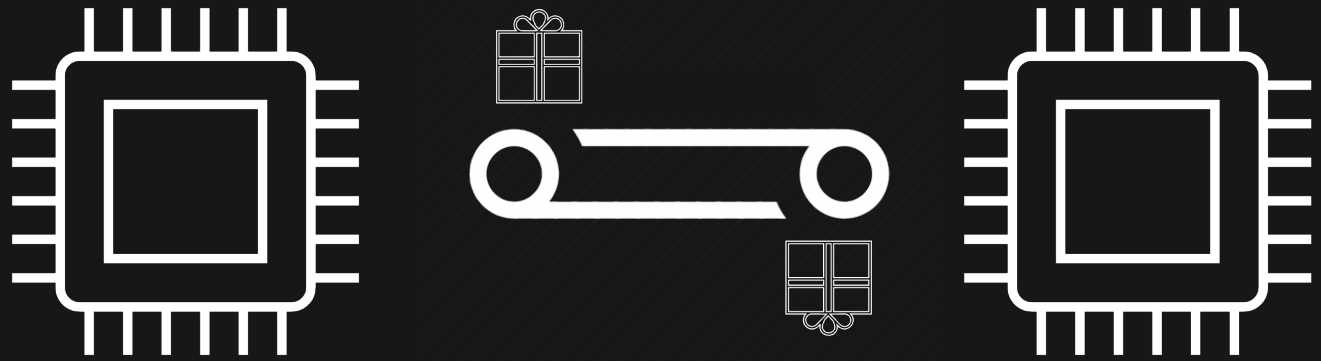
SPI – In general



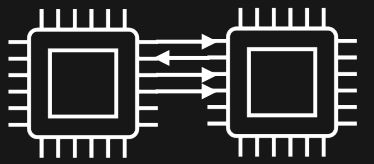
A communication protocol which acts like a conveyer belt

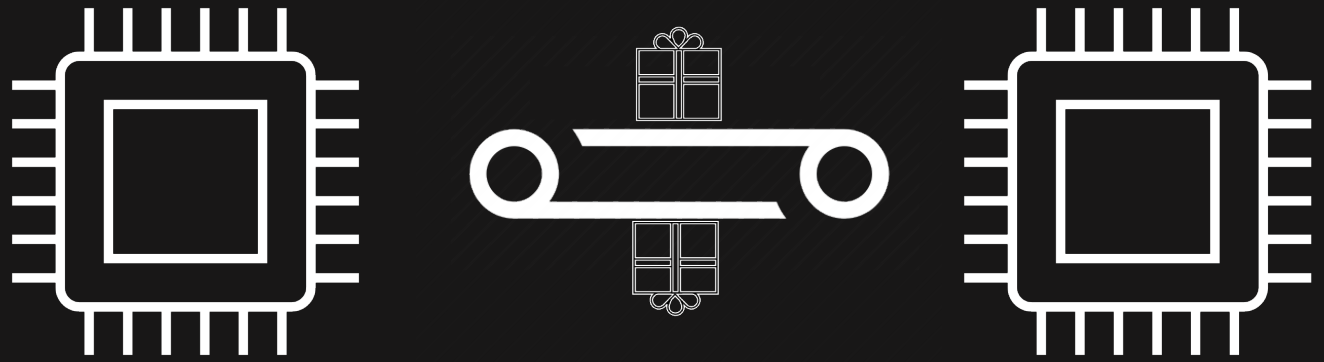
SPI – In general



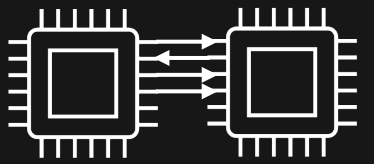


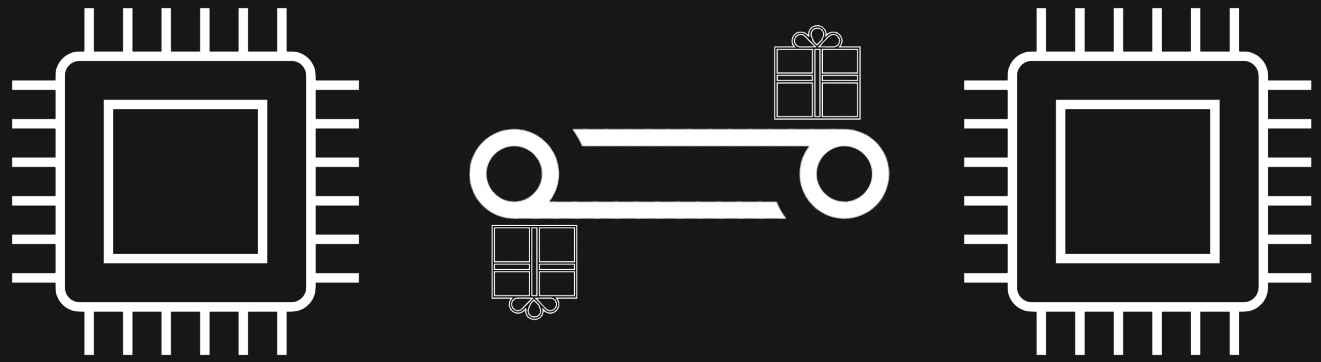
SPI – In general



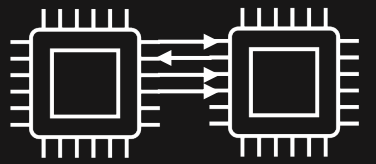


SPI – In general



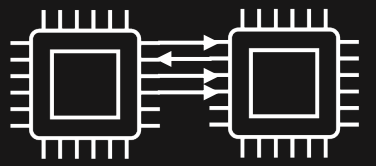


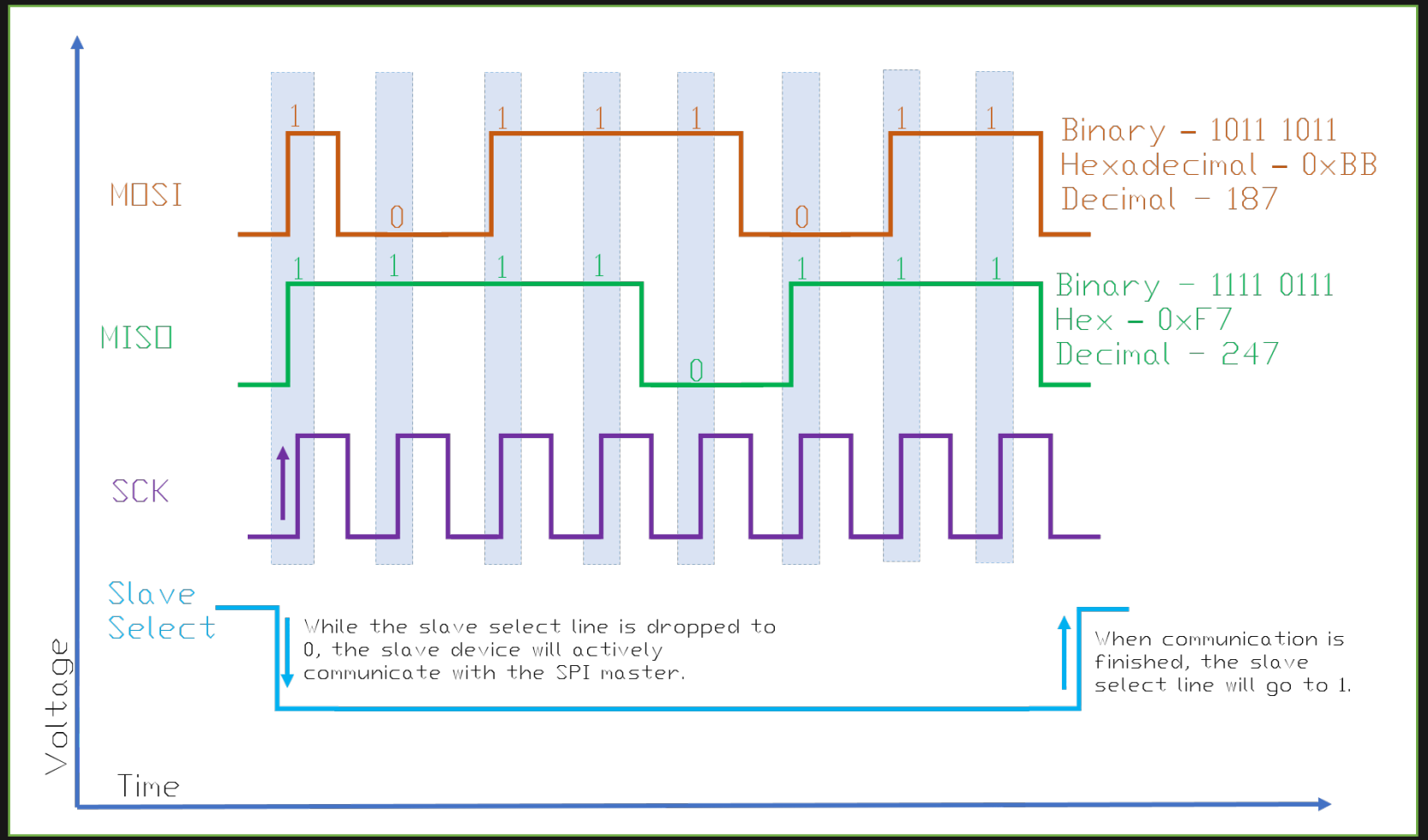
SPI – In general



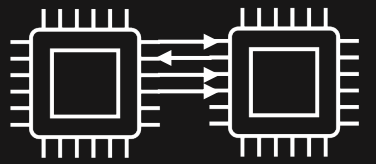
MOSI: Master Out Slave In
MISO: Master In Slave Out
SCK: Clock signal (provided by master)
CS: Chip select (used to notify the slave that we're about to transmit/receive)

SPI – In general



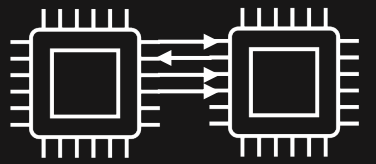


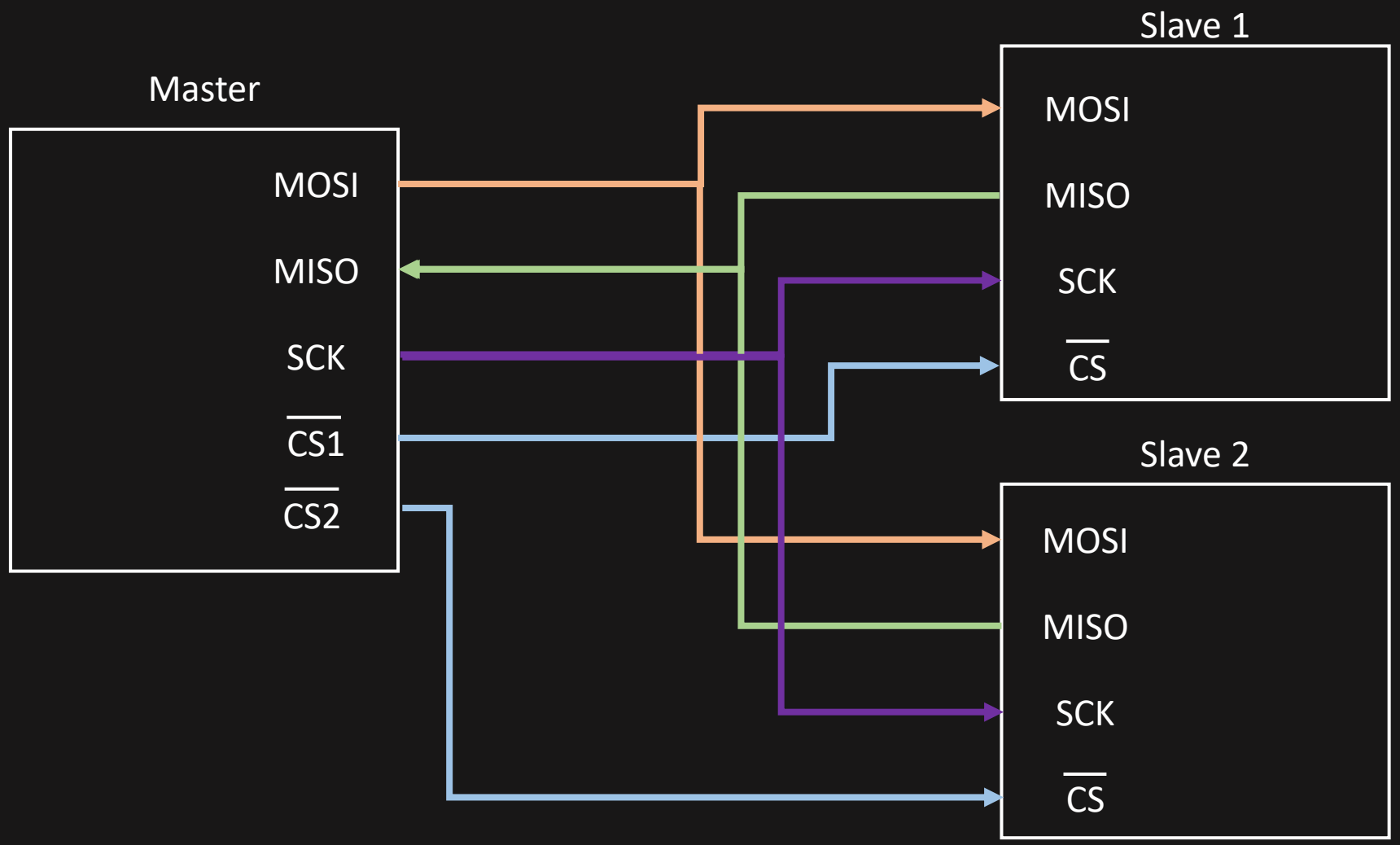
SPI – In general



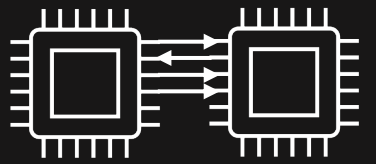
SPI is one to many

SPI – In general



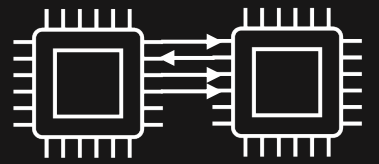


SPI – In general



Why do we care?

SPI – How to set up



1. Set up pins (MOSI, SCK and CS as outputs, MISO as input).
2. Enable the SPI module and set it to master (SPI0.CTRLA register).
3. Make sure chip select does not disable master mode (SPI0.CTRLB, SSD bit).

24.5.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: -

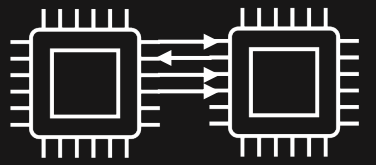
Bit	7	6	5	4	3	2	1	0
		DORD	MASTER	CLK2X		PRESC[1:0]		ENABLE
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

24.5.2 Control B

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	BUFEN	BUFWR				SSD	MODE[1:0]	
Access	R/W	R/W				R/W	R/W	R/W
Reset	0	0				0	0	0

SPI – How to send data



1. Set the chip select low (active low).
2. Fill in the data (SPI0.DATA register).
3. Wait until data is sent.
4. Do a dummy read.
5. Set the chip select high.

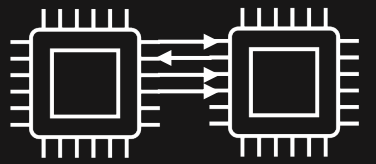
24.5.4 Interrupt Flags - Normal Mode

Name: INTFLAGS
Offset: 0x03
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	IF	WRCOL						
Access	R/W	R/W						
Reset	0	0						

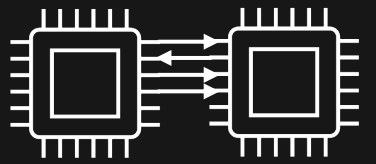
Bit 7 – IF Receive Complete Interrupt Flag/Interrupt Flag
This flag is set when a serial transfer is complete and one byte is completely shifted in/out of the SPIn.DATA register. If $\overline{SS}$ is configured as input and is driven low when the SPI is in Master mode, this will also set this flag. IF is cleared by hardware when executing the corresponding interrupt vector. Alternatively, the IF flag can be cleared by first reading the SPIn.INTFLAGS register when IF is set, and then accessing the SPIn.DATA register.

SPI – Final remarks

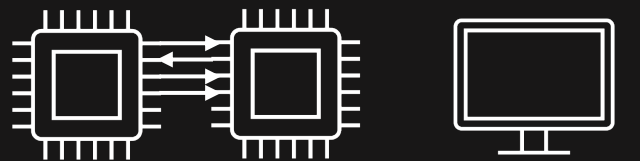


SPI is one of the fastest and simplest protocols out there

SPI



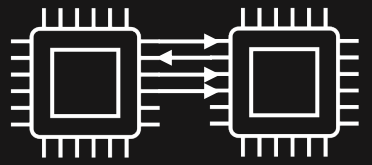
Questions?



SPI

OLED

Task 1



SPI

Analog to digital converter

OLED

Task 2